Impossibility of a pure resistance measurement: The charge-pileup model

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Recently, we have experimentally demonstrated the existence of a capacitance between conductors in the absence of an insulator. We show that a combination of current continuity and Poisson's equation leads to a charge pileup, and thus a capacitance, whenever two dissimilar metals are joined. We verify this with numerical simulations, and consider this intrinsic, inescapable capacitance in the context of Coulomb blockade devices.

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I. MOTIVATION AND INTRODUCTION

The concept of the measurement of a "pure resistor" has a long and venerable history, including in the area of resistance metrology.[1] The general notion of a resistance measurement connotes a circuit with a specific length of metal or semiconductor, defined as the resistor, which is connected by leads typically of other materials or geometry, to an ohm meter or other measurement system. As we will show below, this change in resistivity between the leads and the defined resistor inevitably leads to an inline capacitance that is in parallel with the resistor; this capacitance is directly associated with the interface between the different conductors, as schematically indicated in Fig. 1. Here, the basic concept is: (i) a lower gate voltage raises the conduction band minimum (shown with a nonzero bias voltage) in that area; (ii) this reduces charge density and thus the conductivity in the Si layer; (iii) from current conservation, the reduction in conductivity leads to an increased electric field in the central region (shown by density of arrows in lower section and slope of conduction band minimum in middle section); and (iv) by the Poisson equation, a change in the longitudinal electric field must be produced by a space charge pileup at the edges of the gate region.

It appears to us that the only exception to this intrinsic capacitance would be in measurements of a closed loop, where one might measure the resistance via the capacitively coupled loss in a measurement circuit. In contrast, it does appear possible to have a pure capacitance that has no associated intrinsic resistance, by putting a highly insulating dielectric between the metallic leads.

Until recently, this intrinsic capacitance has not been observable experimentally because in macroscopic objects its magnitude is too small. As an example, if we consider a resistance measurement made by connecting Cu leads to an Evanohm wire wound resistor, 40 gauge wire (0.08 mm diameter) and 1 foot in length, the resistance $R \approx 80\ \Omega$, and $C \approx 10^{-18}$ F. Thus, at any frequency below $1/(2\pi RC) \approx 10^{15}$ Hz, the impedance of this parallel capacitance will be much larger than the resistive impedance; this frequency is independent of length and cross-sectional area.

Recently, through the phenomenon of the Coulomb blockade[2] in single-electron devices, it has become possible and even routine to measure such small capacitances. In particular, in semiconducting single-electron tunneling transistors,[3] it is possible to vary the height of the barrier in the region of reduced conduction (the tunnel junction). In particular, it is possible to reduce the barrier so much that it no longer forms a tunnel junction but is rather a region of reduced semiconductor conductivity separating two regions of larger conductivity. Through Coulomb blockade measurements, we have previously shown it is still possible to measure the capacitance across this region of reduced conductivity.[4] This work naturally raised the question: how is it possible to have capacitance across a region which is not an insulator but rather a conductor? This paper aims to answer that question.

We note that the intrinsic capacitance that we are considering does not correspond to the commonly considered junc-

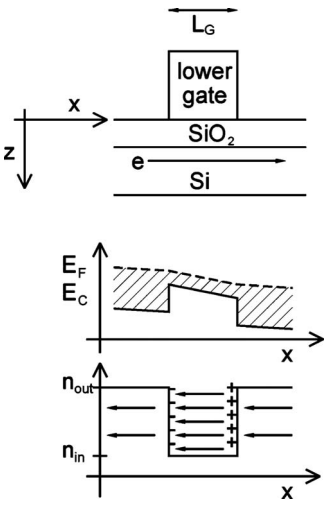

FIG. 1. Upper: schematic of crucial parts of device, with conducting electrons at Si/SiO_2 interface, and a lower gate that inhibits conduction in the region underneath (not shown: upper gate that attracts conducting electrons to interface); middle: band diagram in Si at interface. Conduction band (E_C) and Fermi level (E_F) are tilted more in barrier region, due to lower carrier density and conductivity; bottom: carrier density is lower in the barrier region than outside. Current continuity leads to higher electric field (density of arrows) in the barrier region; change in electric field requires the "charge pileup" as indicated by negative and positive signs at the edges of the barrier region.

tion, depletion, nor metal-oxide-semiconductor capacitance, because all of those three are capacitances across an insulating depletion region. We should note an important similar work,[5] by the CEA group, which studied the capacitance dependence on gate voltage in similar devices. They operated in the regime where the barrier forms a tunnel junction, and not in the regime considered in this paper, where the barrier is even lower and controls a region of classical conduction. This group suggested the change in capacitance was due to enhanced electronic polarizability[5] in the regime of tunneling transport. In this paper, we will present a simple heuristic framework for understanding the intrinsic capacitance in any resistor, present numerical results on a nanotransistor that confirm the basic framework, and compare the model, the numerical results, and the experimental results.

II. MODEL

As described above, the schematic picture in Fig. 1 provides our first answer to the question of how capacitance can develop across a conducting region: the charge piles up at the interfaces between regions of different conductivity. It is also illuminating to consider heuristically how the charge pileup occurs in time, starting from equilibrium, assuming the barrier affects only the carrier density and not the mobility or drift velocity: starting from zero drain voltage and abruptly imposing a nonzero drain voltage: (i) a uniform longitudinal electric field and thus drift velocity leads to a smaller current density $j=nev$ (n, e, and v are the carrier density, electron charge, and drift velocity, respectively) in the barrier region; (ii) the disparities in current densities lead to a buildup of electron charge at the left interface and a concomitant deficit at the right interface; (iii) this extra space charge buildup, through the Poisson equation, leads to an enhanced electric field and thus an enhanced current density in the barrier region; and (iv) this pileup continues until the electric field and drift velocity inside increase enough so that the current density inside matches the current density outside, reestablishing current continuity.

From the abrupt picture illustrated in Fig. 1, we can also obtain a simple qualitative prediction for the barrier capacitance, by generalizing the "Mott-Gurney Square law":[6,7] the current density $j=n_{\mathrm{in}}e\mu E_{\mathrm{in}}=n_{\mathrm{out}}e\mu E_{\mathrm{out}}$, where μ is the mobility (assumed constant in this simple derivation) and E_{in} and E_{out} are the electric fields inside and outside the barrier region. Since the carrier density is lower inside, the electric field must be higher in order to maintain current continuity. From Gauss' law, we have $E_{\mathrm{in}}-E_{\mathrm{out}}=\sigma/\epsilon_{\mathrm{b}}$, where σ and ϵ_{b} are the aereal charge density at the boundary and the bound (not including free-electron contribution) dielectric constant, respectively. It is straightforward to derive that the capacitance due to the charge buildup is

$$C_{\mathrm{B}} = C_{\mathrm{bare}}(1 - n_{\mathrm{in}}/n_{\mathrm{out}}),$$

C_{bare} is the standard geometrical capacitance $C_{\mathrm{bare}}=\epsilon_{\mathrm{b}}A/L_{\mathrm{G}}$, L_{G} and A are the barrier length and the wire cross-sectional area. The two limits of this relation are sensible: for an insulating barrier ($n_{\mathrm{in}} \ll n_{\mathrm{out}}$), the barrier capacitance recovers the standard result; for a single continuous piece of metal ($n_{\mathrm{in}}=n_{\mathrm{out}}$), there are no interfaces and the barrier capacitance collapses to zero.

Given this simple result for the barrier capacitance from the charge pileup model, we can also comment on the quantitative connection between this capacitance value and Coulomb blockade calculations. In general, calculations of Coulomb blockade depend on capacitances through calculations of electrostatic energy embodied in the electric fields in those capacitances. In this context, it is clear from the above that the barrier capacitance that we have proposed corresponds to an electric field inside the barrier region; the existence of this electric field requires energy in just the same way as any other capacitance. Thus, the barrier capacitance considered in this paper will be equivalent to any classical capacitance for calculating Coulomb blockade energetics.

Although heuristically useful, the abrupt picture is unphysical both due to the discontinuities at the interfaces, and because of the artificial separation of the longitudinal (x) and vertical (z) directions. We now consider a toy model which relaxes both of these constraints and which will also allow us to evaluate the results of our numerical simulations. We consider a model with both a lower gate (small positive voltage) and an upper gate (not shown, larger positive voltage) (Ref. 8) which generate an inversion layer at the top surface of the Si in the static case, and add a bias voltage V_{D} across the longitudinal direction for the dynamic case.

Static Case. For the electrostatic potential in the absence of a bias voltage, we have $\phi=\phi_{\mathrm{S}}\{1-\alpha e^{-[(x-x_0)/\delta]^2}\}\ (\frac{z-z_0}{z_0})^2$, where ϕ_{S} is the surface potential at the source and drain, $x_0=50$ nm, $\delta=10$ nm, and $z_0=5$ nm are the center and half width of the barrier region and the vertical extent of the inversion layer, and $\alpha=1/3$ is the fractional size of the barrier, with typical values listed; x and z are as defined in Fig. 1. The vertical (z) parabolic dependence is the typical one for an inversion layer[9] leading to a constantly decreasing vertical electric field E_z from 0 to z_0, and a constant negative space charge over the same region. This negative space charge balances the positive charge on the lower gate and the upper gate which produce the inversion layer. The longitudinal (x) dependence produces a longitudinal electric field in the Si pointing inward from the upper gate on both sides toward the barrier region underneath the less positively biased lower gate.

Dynamic Case. In order to examine the charge pileup in our toy model, we need to impose a longitudinal bias voltage drop, V_{D}. Since we can examine in detail the results of the realistic numerical simulations in the next section, for our toy model we have chosen a simple prescription which allows us to examine the x and z dependences of the potential, electric field, and space charge: rather than include resistivity and current, we simply impose an electrostatic potential that mimics the voltage drop, and then examine the consequences of that choice.

In Poisson's equation, $-\nabla^2\phi=\nabla\cdot\vec{E}=\partial E_x/\partial x+\partial E_y/\partial y+\partial E_z/\partial z=\rho/\epsilon_{\mathrm{b}}\equiv(\rho_x+\rho_y+\rho_z)/\epsilon_{\mathrm{b}}$, with $\vec{E}$, E_{i} the electric field vector and its components, ρ the space charge density, and where we have defined ρ_i to be the terms in the space charge density corresponding to the partial derivatives of the electric

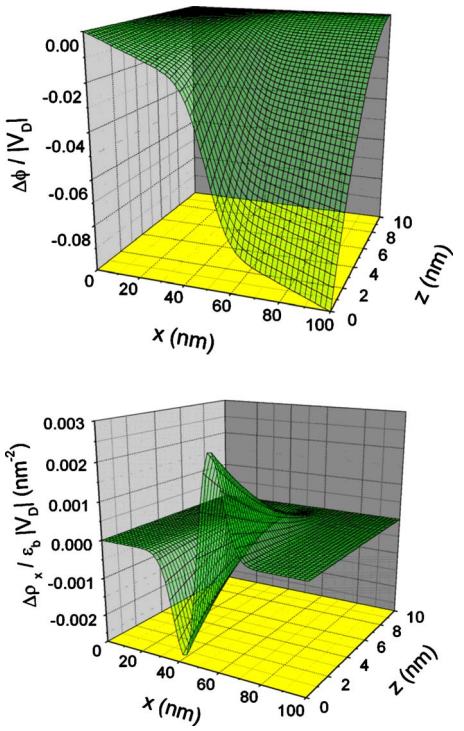

FIG. 2. (Color online) Upper: change in electrostatic potential due to imposition of bias voltage; note that potential drops off along x direction more rapidly in barrier region and that modulation falls off quadratically in z direction. Lower: change in space charge density $\Delta\rho_x$ due to imposition of bias voltage. Note positive and negative charge lobes which generate the electric fields and the electrostatic potential change shown in the upper part, and that the modulation falls off quadratically in the z direction.

field. From the linearity, we can define $\Delta\phi$, $\Delta\vec{E}$, $\Delta\rho$ to be the changes in these quantities due to the imposition of a longitudinal bias voltage.

The potential change is $\Delta\phi = -|V_D|\{\beta/2[1+\mathrm{erf}[(x-x_0)/\delta]]+(1-\beta)x/L\}(\frac{z-z_0}{z_0})^2 \equiv -|V_D|\Delta\mathcal{X}(x)\mathcal{Z}(z)$, where $L=100$ nm is the length of the device and $\beta(V_{LG})=0.6$ represents the fraction of the total voltage drop V_D across the barrier region; this fraction corresponds to the larger resistivity in this region and contains the dependence on the gate voltage V_{LG}. $\Delta\phi$ is shown in Fig. 2, upper with the barrier region from 40 to 60 nm.

Following Poisson's equation, we obtain a change in space charge density $\Delta\rho/\epsilon_b = |V_D|\{\beta\mathcal{Z}(z)e^{-[(x-x_0)/\delta]^2}\frac{x-x_0}{\delta}\frac{1}{\delta^2} - 2\Delta\mathcal{X}(x)\frac{1}{z_0^2}\} \equiv (\Delta\rho_x+\Delta\rho_z)/\epsilon_b$. The second term $\Delta\rho_z/\epsilon_b$ is uniformly negative and acts to balance the additional positive charge on the gates induced by the negative potential change $\Delta\phi$. The first term $\Delta\rho_x/\epsilon_b$ has extrema ($z=0$) at $x = x_0 \pm \delta/\sqrt{2}$ of magnitude $\mp|V_D|\frac{e^{-1/2}}{\sqrt{2}}\frac{\beta}{\delta^2} \approx \mp|V_D|\frac{1}{4\delta^2}$. The negative and positive lobes in $\Delta\rho_x$ generate the longitudinal electric field E_x that points toward the barrier region from both sides, and thus generates the extra potential drop $\Delta\phi$ in the barrier region; $\Delta\rho_x$ is shown in Fig. 2, lower. This toy model also demonstrates that, as assumed in the abrupt picture discussed above, it is sensible to separate out the x and z dependences.

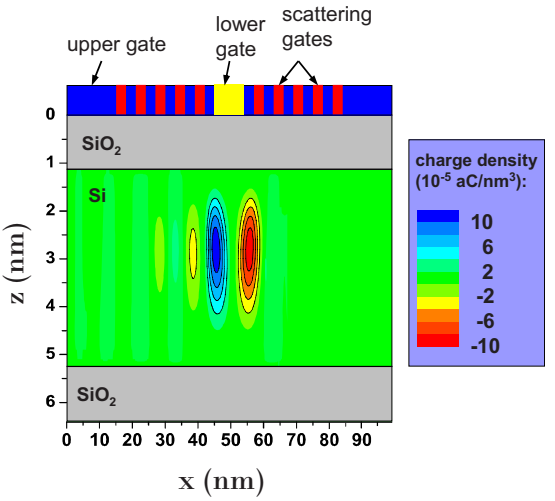

FIG. 3. (Color online) Schematic of device geometry for simulations and simulation result. The schematic shows both the top gate oxide SiO_2 as well as the 4 nm deep active Si layer. The upper gate and scattering gates provide the conducting electron gas, as well as the finite conductivity outside the lower gate region. The terminology of "upper" and "lower" gates refers to the fact (not shown in Fig. 3) that in the actual devices, the upper gate is deposited everywhere, and sits on top of the lower gate (with an insulating layer in between). By biasing the lower gate to a more negative voltage, the region underneath the lower gate has a lower carrier density and conductivity, thus providing the barrier region. In the Si region, we show contours of constant charge density $\Delta\rho$ as generated by the bias voltage V_D. The positive and negative charge lobes demonstrate the basic result of this work: capacitive charge buildup across the barrier region, even when about half of the transport occurs via classical over-the-barrier transport.

Having demonstrated the basic qualitative results of this toy model, we can also now derive a prediction for the dependence on gate voltage, which we can use when interpreting the results of the numerical simulations. We estimate Q_{lobe} by multiplying a volume $\Omega = \delta\Delta y z_0 = \delta A$ by the maximum $\Delta\rho_x = \epsilon_b|V_D|\frac{e^{-1/2}}{\sqrt{2}}\frac{\beta}{\delta^2}$ to obtain $Q_{lobe} = \Omega\Delta\rho_x \approx \frac{1}{2}|V_D|\frac{\epsilon_b A}{\delta}\beta(V_{LG})$ or $C_B = Q_{lobe}/|V_D| \approx C_{bare}\beta(V_{LG})$. Finally, at the surface $z=0$, $(1/|V_D|)\partial\Delta\phi/\partial x \approx (1-\beta)/L, \beta/2\delta+(1-\beta)/L$ outside and inside the barrier region, respectively. From this, we obtain

$$\beta \approx \frac{\frac{\Delta V_{in}}{V_D} - \frac{d}{L}}{1-\frac{d}{L}}, \quad C_B \approx C_{bare}\frac{1}{\left(\frac{L}{d}-1\right)\frac{n_{in}}{n_{out}}+1}\left(1-\frac{n_{in}}{n_{out}}\right), \tag{1}$$

where $d=2\delta$ is the length of the barrier region. Note that the result for C_B is very similar to the abrupt picture result.

III. NUMERICAL SIMULATIONS

Incorporating the important features of our measured device,[8] the device as modeled is indicated in Fig. 3. The source and drain regions ($x<0$ and $x>99$) are regions of

infinite conductivity in the Si. By applying positive voltage to the upper gate, we attract electrons to the Si/SiO_2 interface, thus turning on conduction in the Si. The simulation does not include bulk Si scattering; thus, in order to get a finite conductivity in the conducting region outside the barrier, we introduce scattering gates, which have a less positive voltage than the upper gate. The central lower gate (middle gate, highlighted in yellow online) has a voltage V_{LG} applied to it; since $V_{LG} < V_{UG}$, the barrier region underneath the lower gate has a lower carrier density and thus conductivity than the region outside.

We now turn to the results of our numerical simulations. These fully charge self-consistent quantum transport simulations used a very efficient implementation of the nonequilibrium Green's function formalism,[10] termed the Contact Block Reduction (CBR) method.[11,12] The CBR method rigorously separates the open system problem into the solution of a suitably defined closed system (energy-independent) eigenproblem and the energy-dependent solution of a small linear system of equations of size determined by the contact regions that couple the closed system to the leads. Calculations of the current and charge density of the open system throughout the device are performed with an effort comparable to a single calculation of a small percentage of the eigenstates of a closed system.[13] The charge self-consistency is achieved using the predictor-corrector approach as described in Ref. 13. In our simulations an electrostatic potential error tolerance of $\pm 10^{-7}$ eV was obtained within six to ten iterations. Such a low error tolerance was essential for accurate calculation of the capacitive charge distribution, i.e., the small difference in the charge density due to the applied drain bias.

Figure 3 also shows the main simulation result for this work: positive (blue) and negative (red) charge lobes (total magnitude of order 10 aC, corresponding to a few percent of the static charge density generated by the gate voltages) appear on either side of the barrier region underneath the lower gate.[14] It is particularly important to note that the simulation was done at a gate voltage of $V_{LG} = -0.04$ V, when almost half of the transport is classical over the barrier and not tunneling, and where the ratio of $n_{out}/n_{in} \approx 3$. This simulation result confirms that there can be a capacitance in the absence of a pure tunneling barrier, or to put it a different way, that this system cannot be viewed as a "pure" resistor.

Having demonstrated the basic existence of capacitive charge lobes for classical over-the-barrier transport, Fig. 4 allows elucidation of some of the underlying physics. The inset shows that, over the entire range of lower gate voltages used in the simulation, a substantial fraction of the transport is over the barrier, as opposed to tunneling under the barrier. This fraction is calculated by observing that the energy spectrum of transport (not shown) contains two peaks at about −0.01 eV (tunneling) and −0.002 eV (over-the-barrier), integrating the area under both peaks, and taking the ratio. The main part of the figure shows the dependence of the calculated barrier capacitance C_B on the lower gate voltage; as predicted qualitatively by the models considered above, the charge pileup and the capacitance decrease as the lower gate voltage becomes less negative, because the carrier density and conductivity in the barrier region are getting closer to those outside. In addition, we show the dependence of β as well, as calculated from Eq. (1); the similar dependences of C_B and β show that the charge pileup underlies the simulation results.

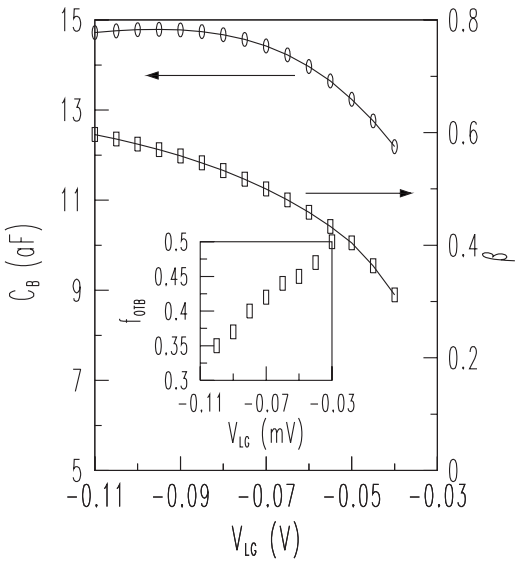

FIG. 4. From numerical simulations at $T = 10$ K. Inset: fraction of transport over the barrier, versus tunneling under the barrier, as a function of the lower gate voltage. Main: capacitance ($C_B \equiv Q_{lobe}/V_D$) and β as a function of lower gate voltage V_{LG}. As the gate voltage becomes less negative, the carrier density and conductivity inside the barrier region increase, and thus the charge pileup decreases, in agreement with the numerical simulations; this agreement is also indicated by the similarity of the dependence of $\beta(V_{LG})$.

Finally, we can compare our simulation results to the experimental results (Fig. 4 of Ref. 4). We note first that the simulation results are in quite good quantitative agreement with the data, which shows a range of capacitance values $C_B \in [15,23]$ aF. In addition, over the experimental voltage range (this range differs markedly from our simulation results, due to work function differences which are not considered in the numerical simulations) from −1.9 to −1.85 V, C_B falls off by about a factor of 1/3, in good agreement with the numerical results. We note that this decrease is opposite in direction to that predicted by the electronic polarizability model.[5] The experimental value of the barrier capacitance increases quite markedly at even less negative finger gate voltages, presumably because either (i) the enhanced electronic polarizability[5] becomes dominant here or (ii) as in Ref. 4, the physical width of the barrier region is decreasing as we continue to make the finger gate voltage less negative. In terms of the model, if possibility (ii) is correct, it appears that the dominant effect in this higher gate voltage range is to increase the value of C_{bare}.

IV. CONCLUSIONS

In previous work, starting from measurements of the barrier capacitance in a Coulomb blockade device,[4] we have experimentally measured a barrier capacitance even in a re-

gime where there is no insulating barrier. In this work, we have shown that a simple model, confirmed by simulations, gives an answer to this conundrum: consideration of current continuity plus Poisson's equation yields the fact that a "pure resistance" does not exist; there is always a parallel capacitance which is immeasurably small except in Coulomb-blockade devices.

Following on from this, we can ask the question: why is there still Coulomb blockade in a device which has no insulating barrier? The answer to this question is beyond the scope of this paper and some of the issues have been discussed previously.[15–17] One critical question is whether electrons transport across the barrier region as discrete particles or in a continuous fluid. In particular, we note that the average number of electrons in the barrier region in our devices at any instant in time is substantially less than one, even when the device is far into the classical over-the-barrier transport regime. We suggest that this parameter may indeed be the relevant one for the crossover from discrete particle transport to a continuous fluid. Finally, we can comment on an application, as discussed in Ref. 4: by confirming the charge pileup model, we have strengthened the possibility of elucidating the shape and size of barrier regions electrostatically produced in these Si nanowires, which will be of great importance as we move forward with using these for various applications.

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